DOUBLE DATA RATE MEMORY DEVICES INCLUDING CLOCK DOMAIN ALIGNMENT CIRCUITS AND METHODS OF OPERATION THEREOF

ABSTRACT OF THE DISCLOSURE

An integrated circuit memory device includes a memory, a read control circuit operatively associated with the memory and configured to produce data from the memory responsive to an externally-applied input clock signal, and an output latch configured to transfer data at an input thereof to an output pad of the memory device responsive to an externally-applied output clock signal. The device further includes a clock domain alignment circuit configured to receive the data produced by the memory and to responsively provide the data at the input of the output latch based on relative timing of the input clock signal and the output clock signal.